REMARKS

This Application has been carefully reviewed in light of the Office Action mailed April 5, 2004. Applicant appreciates the Examiner's consideration of the Application. Claims 1, 8, 15, and 22 have been amended to clarify, more particularly point out, and more distinctly claim inventive concepts previously present in these claims. Applicant makes no admission that these amendments narrow the scope of the claims or that the amendments are required for patentability. Applicant respectfully submits that no new matter has been added by the amendments to the claims. In order to advance prosecution of this Application, Applicant has responded to each notation by the Examiner. Applicant respectfully requests reconsideration and favorable action in this case.

Telephone Interview

Applicant thanks the Examiner for the courtesy of the telephone interview conducted on July 1, 2004. The substance of the interview was a discussion of the rejection of Claims 1-22 under 35 U.S.C. §§ 112 and 103. The Examiner conditionally agreed to withdraw the rejection under § 112, pending receipt of this Response. The Examiner agreed to review the rejection under § 103 in light of the discussion, but no final agreement was reached on the rejection under § 103.

Section 112 Rejection

The Examiner rejects Claims 1-22 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Applicant respectfully traverses this rejection and certain characterizations or limitations of the terms made by the Examiner. Claims 1-22 are directed towards estimating interconnect delay. Thus, the specification is neither incomplete nor inaccurate by stating that for one embodiment, "Nodes 106 represent elements such as transistors of an integrated circuit," or by using for one embodiment a transfer function $H(s)$ calculated using the inductance of an interconnect. (Specification, page 6, lines 14-15; page 9, line 23 to page 10, line 16.)

Accordingly, the specification contains a written description of the invention to enable one skilled in the art to make and use the claimed invention. Applicant respectfully requests the Examiner to withdraw the rejections of Claims 1-22 under 35 U.S.C. § 112.

Section 103(a) Rejection

The Examiner rejects Claims 1-22 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,379,231 to Pillage al. ("*Pillage*"). Applicant respectfully traverses this rejection for the reasons discussed below.

Applicant respectfully submits that *Pillage* fails to disclose, teach, or suggest elements specifically recited in Applicant's claims. For example, *Pillage* fails to disclose, teach, or suggest:

(1) "determining a transfer function using the interconnect inductance";

(2) "estimating an interconnect response using the two poles, the interconnect response describing a reaction of the interconnect to an applied signal"; and

(3) "estimating an interconnect delay from the interconnect response, the interconnect delay describing a delay of the interconnect" (recited in independent Claim 1).

Pillage discloses a "method and apparatus for simulating a microelectronic circuit or system." (*Pillage*, Abstract.) According to *Pillage*:

> As shown in Block 30, the stored representation of the RLC interconnect circuit is transformed into an equivalent DC circuit. As shown in Block 40, the equivalent DC circuit is then converted into a directed graph and a spanning tree is constructed from the directed graph at Block 50. The spanning tree is then traversed at Block 60. If there are no resistor loops present in the circuit, the next generation of moments is computed at Block 70. The moments are then mapped to the dominant time constants in Block 80 using either a constrained approximation or a preferred moment shifting technique.

(*Pillage*, column 7, lines 27-38.)

> The stored circuit representation is then transformed to its equivalent DC circuit, Block 30, by replacing all capacitors with current sources and all inductors with voltage sources. The transformed circuit is shown in FIG. 18(b). A linear passive RLC circuit, when transformed, contains only independent voltage sources, independent current sources, and resistors, regardless of the topology.

(*Pillage*, column 9, lines 30-37.) *Pillage* also discloses, "After the circuit graph and spanning tree are constructed, a path tracing procedure or traversal is used to generate a set of circuit moments; two moments are required for each model order. (*Pillage*, column 13, lines 14-17.)

Applicant respectfully submits that *Pillage* fails to disclose, teach, or suggest elements specifically recited in Claim 1. First, as shown above, *Pillage* discloses transforming a circuit representation by replacing all capacitors with current sources and all inductors with voltage sources. Accordingly, *Pillage* fails to disclose, teach, or suggest "determining a transfer function using the interconnect inductance," recited in Claim 1. For at least this reason, Claim 1 is patentable over *Pillage*.

Second, as shown above, *Pillage* discloses that a spanning tree is constructed from the circuit representation, and a path tracing procedure or traversal is performed on the spanning tree to generate a set of circuit moments. Accordingly, *Pillage* fails to disclose, teach, or suggest "estimating an interconnect response using the two poles, the interconnect response describing a reaction of the interconnect to an applied signal," and "estimating an interconnect delay from the interconnect response, the interconnect delay describing a delay of the interconnect," recited in Claim 1.

Consequently, at a minimum, *Pillage* fails to disclose, teach, or suggest the elements specifically recited in independent Claim 1, whether *Pillage* is considered alone or in combination with statements relied on by the Examiner.

Applicant's dependent claims are allowable based on their dependence on the independent claim and further because they recite numerous additional patentable distinctions over the reference of the rejection. Because Applicant believes he has amply demonstrated the allowability of the independent claim over the reference of the rejection, and to avoid burdening the record, Applicant has not provided detailed remarks concerning these dependent claims. Applicant, however, remains ready to provide such remarks if it becomes appropriate to do so.

Applicant respectfully requests reconsideration and allowance of independent Claim 1 and all claims that depend on Claim 1.

Independent Claims 8, 15, and 22 recite certain limitations substantially similar to those recited in independent Claim 1. Accordingly, for at least the same reasons, Applicant also respectfully requests reconsideration and allowance of independent Claims 8 and 15, together with their dependent claims, and independent Claim 22.

CONCLUSION

Applicant has made an earnest attempt to place this case in condition for allowance. For at least the foregoing reasons, Applicant respectfully requests full allowance of all the pending claims.

If the Examiner believes a telephone conference would advance prosecution of this case in any way, the Examiner is invited to contact Keiko Ichiye, the Attorney for Applicant, at the Examiner's convenience at (214) 953-6494.

Although Applicant believes no fees are due, the Commissioner is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 02-0384 of Baker Botts L.L.P.

Respectfully submitted,

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